



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/736,838

12/17/2003

Hee-Kwan Son

8947-000062/US

5435

30593

7590

11/25/2008

HARNESS, DICKEY & PIERCE, P.L.C.

P.O. BOX 8910

RESTON, VA 20195

EXAMINER

ALMEIDA, DEVIN E

ART UNIT

PAPER NUMBER

2432

MAIL DATE

DELIVERY MODE

11/25/2008

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/736,838	<b>Applicant(s)</b> SON, HEE-KWAN	
	<b>Examiner</b> DEVIN ALMEIDA	<b>Art Unit</b> 2432	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 28 July 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 8-53 is/are pending in the application.
- 4a) Of the above claim(s) 39-52 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 8, 11-16, 19, 21-23, 26, 30-35, 38 and 53 is/are rejected.
- 7) ☒ Claim(s) 9, 10, 17, 18, 20, 24, 25, 27-29, 36 and 37 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

### **DETAILED ACTION**

This action is in response to the papers filed 1/16/2008. In response to the restriction requirement applicant elects with traverse to claims 1-38 and 53 were received for consideration.

#### ***Response to Arguments***

Applicant's arguments have been fully considered but they are not persuasive. The output of Multiplier 164 does input into General Purpose Register 119. No where in the claims does it say that it has to be a direct input to a register.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., that the arithmetic unit 111 does not deal with data--such as a multiplicand, multiplier, or modulus---and, thus, is not a modulus recoder. For similar reasons, instruction address register 147 is not a modulus feedback register.) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Since Modulus recoder does not have a common meaning in the art and the specification does not specify to one what a modulus recoder is an Address arithmetic unit is functionally equivalent.

Applicant's arguments have been fully considered but they are not persuasive. With respect to claim 8 Essig shows a modulus recoder (see figure 1 element 111); a multiple modulus synch register (see figure 1 element 147); wherein an input to the multiple modulus synch register is at least one output from the modulus recoder (see figure 1 the modulus recoder (i.e. element 111) inputs to multiple modulus synch register (i.e. element 147)).

Applicant's arguments have been fully considered but they are not persuasive. With respect to claim 11 Essig shows a modulus recoder (see figure 1 element 111); a modulus feedback register (see figure 1 element 147); wherein an input to the modulus feedback register is at least one output from the modulus recoder (see figure 1 the modulus recoder (i.e. element 111) inputs to multiple modulus synch register (i.e. element 147)) and wherein an input to the booth register (see figure 1 element 119) is at least one output from the booth recoder (see figure 1 element 164 and column 5 lines 1-50).

Applicant's arguments have been fully considered but they are not persuasive. With respect to claim 19 Essig teaches a mux (see figure 1 element 157 multiplexer); wherein the booth recoder and the mux are used to obtain a partial product (see figure 1, figure 3 and column 5 lines 1-50).

Applicant's arguments have been fully considered but they are not persuasive. With respect to claim 26 Essig teaches a modulus recoder (see figure 1 element 111); wherein the modulus recoder generates a current multiple modulus selection signal unless an enabling signal has a predetermined value, if the enabling signal has a predetermined value, a previous value of the selection signal is used without generating a multiple modulus selection signal, the selection signal is used to select a multiple modulus value (see column 3 line 9 – 66 and column 5 lines 1-50).

Applicant's arguments have been fully considered but they are not persuasive. With respect to claim 30 Essig teaches wherein an input to the booth synch register (see figure 1 element 119) is at least one output from the booth recoder (see figure 1 element 164 and column

Art Unit: 2432

5 lines 1-50); wherein an input to the booth register (see figure 3 element 229) is at least one output from the booth recoder (see figure 1 element 164 and column 5 lines 1-50).

Applicant's arguments have been fully considered but they are not persuasive. With respect to claim 53 Essig teaches means for modulus storing, wherein the means for modulus storing stores at least one output value from a modulus recoder (see figure 1 element 111)

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 8, 11-16, 19, 21, 26, 30-35, 38 and 53 are rejected under 35 U.S.C. 102(b) as being anticipated by Essig et al (U.S. 4,646,257).

With respect to claim 8, a multiplier, comprising: a booth recoder (see figure 1 element 164 and figure 3 element 217 column 5 lines 1-50); a partial product synch register (see figure 3 element 189), a modulus recoder (see figure 1 element 111); and

a multiple modulus synch register (see figure 1 element 147), wherein an input to the partial product synch register is at least one output from the booth recoder (see figure 3); wherein an input to the multiple modulus synch register is at least one output from the modulus recoder (see figure 1 element 147), where the partial product synch register and the multiple modulus synch register are used to synchronize signals derived from the outputs of the booth recoder and the modulus recoder (see column 3 line 9 – 66 and column 5 lines 1-50).

With respect to claim 11, a multiplier, comprising: a modulus recoder (see figure 1 element 111); a modulus feedback register, wherein an input to the modulus feedback register is at least one output from the modulus recoder (see figure 1 element 14); a Booth recoder (see figure 1 element 161 and figure 3 element 217 column 5 lines 1-50); and a booth register, wherein an input to the booth register is at least one output from the booth recoder (see figure 1 element 119 and column 5 lines 1-50), where the modulus feedback register and the booth register save values enabling decreased computation power usage in the multiplier (see column 3 line 9 – 66 and column 5 lines 1-50).

With respect to claim 12, wherein the booth register is a feedback register that stores at least one output value of the booth recoder to be fed back to the booth recoder (see figure 1 element 119 and column 5 lines 1-50).

With respect to claim 13, wherein the output value is a partial product selection signal, where the partial product selection signal is used to select a partial product value (see figure 3).

With respect to claim 14, wherein the booth register is a pipeline register, the pipeline register stores output values of the booth recoder (see figure 3).

With respect to claim 15, wherein the modulus feedback register stores at least one output value of the modulus recoder to be fed back to the modulus recoder (see figure 1 element 14).

With respect to claim 16, wherein the output value is a multiple modulus selection signal, where the multiple modulus selection signal is used to select a multiple modulus value (see column 3 line 9 – 66).

With respect to claim 19, a partial product generator (see figure 1B), comprising: a booth recoder (see figure 3 element 217 column 5 lines 1-50); and a mux (see figure 1 element 165),

Art Unit: 2432

wherein the mux inputs at least one output from the booth recoder, wherein the booth recoder and the mux are used to obtain a partial product (see figure 1).

With respect to claim 21, wherein the booth recoder generates a partial product selection signal and a bit pattern is assigned to any value of the partial product selection signal that is prohibited based on a previous value of the partial product selection signal (see figure 3).

With respect to claim 26, a multiple modulus generator, comprising: a modulus recoder (see figure 1 element 111); and a mux (see figure 1 element 145), wherein the modulus recoder generates a current multiple modulus selection signal unless an enabling signal has a predetermined value, if the enabling signal has a predetermined value, a previous value of the selection signal is used without generating a multiple modulus selection signal, the selection signal is used to select a multiple modulus value (see column 3 line 9 – 66 and column 5 lines 1-50).

With respect to claim 30, a multiplier, comprising: a modulus recoder (see figure 1 element 111); a modulus feedback register, wherein an input to the modulus feedback register is at least one output from the modulus recoder (see figure 1 element 147); a modulus synch register, wherein an input to the modulus synch register is at least one output from the modulus recoder (see figure 1 element 153); a booth recoder (see figure 1 element 161 and figure 3 element 217 column 5 lines 1-50); a booth synch register, wherein an input to the booth synch register is at least one output from the booth recoder (see figure 1 element 119 and column 5 lines 1-50); and a booth register, wherein an input to the booth register is at least one output from the booth recoder (see figure 1 element 119 and column 5 lines 1-50), where the modulus feedback register and the booth register save values enabling decreased computation power

Art Unit: 2432

usage in the multiplier, and where the booth synch register and the modulus synch register are used to synchronize signals derived from the outputs of the booth recoder and the modulus recoder to decrease glitches (see column 3 line 9 – 66 and column 5 lines 1-50).

With respect to claim 31, wherein the booth register is a feedback register that stores at least one output value of the booth recoder to be fed back to the booth recoder (see figure 1 element 119 and column 5 lines 1-50).

With respect to claim 32, wherein the output value is a partial product selection signal, where the partial product selection signal is used to select a partial product value (see figure 3).

With respect to claim 33, wherein the booth register is a pipeline register, the pipeline register stores output values of the booth recoder (see figure 1 and 3).

With respect to claim 34, wherein the modulus feedback register stores at least one output value of the modulus recoder to be fed back to the modulus recoder (see figure 1 element 14).

With respect to claim 38, wherein a multiple modulus value and a partial product value are synchronized by using values from the modulus synch register and values from the booth synch register (see column 3 line 9 – 66 and column 5 lines 1-50).

With respect to claim 53, a Montgomery multiplier comprising; means for inputting, wherein the means for input, enters the values for a modulus, multiplicand, and a multiplier (see abstract); means for booth storing, wherein the means for booth storing stores at least one output value from a booth recoder (see figure 1 element 161 and figure 3 element 217 column 5 lines 1-50); means for modulus storing, wherein the means for modulus storing stores at least one output value from a modulus recoder (see figure 1 element 111); means for partial product generation, wherein the means for partial product generation produces a partial product value using the input



Art Unit: 2432

from the means for input (see figure 3); means for multiple modulus generation, wherein the means for multiple modulus generation produces a multiple modulus value using the input from the means for input (see figure 1); means for synchronizing, wherein the means for synchronizing synchronizes the partial product value and the multiple modulus value (see column 3 line 9 – 66 and column 5 lines 1-50); and means for accumulating, wherein the means for accumulating inputs the synchronized partial product value and the multiple modulus value and produces a result for the Montgomery multiplier (see column 3 line 9 – 66 and column 5 lines 1-50).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 22 and 23 rejected under 35 U.S.C. 103(a) as being unpatentable over Essig et al (U.S. 4,646,257) in view of Takano et al (US 5,790,874). Abbott teaches everything with respect to claim 21 above but does not teach with respect to claim 22, wherein the bit pattern is chosen so that the hamming distance between the current value of the partial product selection signal and the previous value of the partial product selection signal is reduced. Takano teach with respect to claim 22, wherein the bit pattern is chosen so that the hamming distance between the current value of the partial product selection signal and the previous value of the partial product selection signal is reduced (see Abstract). It would have been obvious at the time the invention

Art Unit: 2432

was made to a person having ordinary skill in the art to which said subject matter pertains to have reduced the hamming distance to reduce the power consumption needed to perform the action (see Abstract). Therefore one would have been motivated to have reduced the hamming distance between bit sequences.

With respect to claim 23. The partial product generator of claim 21, wherein the bit pattern is chosen so that the average temporal hamming distance between the current value of the partial product selection signals and their corresponding previous values are reduced (see Abstract).

### ***Allowable Subject Matter***

Claims 9, 10, 17, 18, 20, 24, 25, 27-29, 36 and 37 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Devin Almeida whose telephone number is 571-270-1018. The examiner can normally be reached on Monday-Thursday from 7:30 A.M. to 5:00 P.M. The examiner can also be reached on alternate Fridays from 7:30 A.M. to 4:00 P.M.

Art Unit: 2432

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gilberto Barron, can be reached on 571-272-3799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Devin Almeida/  
Examiner, Art Unit 2432  
10/28/2008

/Benjamin E Lanier/  
Primary Examiner, Art Unit 2432